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First, as shown in FIG. 4A, an insulating film (SiO_2 film) 2 having a thickness of from 100 to 200 nm is formed over the surface of a silicon substrate 1 by or CVD.

As shown in FIG. 4B, an opening is formed for a base electrode of the bipolar transistor. Reference numeral 2a indicates an opening side wall. A p-type polysilicon (poly-Si) film 3 having a thickness of from 100 to 200 nm is formed over the surface by CVD. The p-type poly-Si film 3 serves as a base electrode. It is to be noted that the doping of a p-type impurity to the poly-Si can be also performed by ion implantation.

Next, as shown in FIG. 4C, an insulating film (SiO_2 film) 4 having a thickness of from 300 to 400 nm is formed over the surface of the wafer by CVD, and then an opening 10 for forming an emitter and a base is formed by dry etching, of the laminated films, the SiO_2 film 4 and the p-type poly-Si film 3. After that, an insulating film (SiO_2 film) 5 having a thickness of from 10 to 20 nm is formed over the surface by CVD, and a p-type impurity diffusion layer 6 is formed by ion implantation through the SiO_2 film 5. In this case, for example, ions of BF_3 are implanted in a dose of from 1×10^{13} to $1 \times 10^{14} \text{ cm}^{-2}$ at an implantation energy of from 20 to 30 KeV. The p-type impurity diffusion layer 6 serves as the base, and the

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SiO₂ film 5 having a thickness of from 10 to 20 nm serves as a buffer layer for preventing a channeling tail upon ion implantation for forming the base. The ion implantation is followed by heat-treatment (annealing) for 10 to 20 minutes at 900°C, to form a P⁺ contact layer (graft contact) 3a in the silicon substrate 1 by diffusion from the p-type poly-Si film 3.

Next, as shown in FIG. A, a side wall forming insulating film (SiO₂ film) 7 having a thickness of from 400 to 600 nm is formed over the surface by CVD. The SiO₂ film 7 is then removed by anisotropic etching such as RIE so as to form side walls 7a made of the SiO₂ film in the opening for forming an emitter and a base, as shown in FIG. 5B. The side wall 7a has a function of isolating the base electrode made of the p-type poly-Si film 3 from an emitter electrode which will be formed later. --

Please replace the paragraph beginning at page 4, line 14, with the following rewritten paragraph:

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-- In the bipolar transistor having the above-described base-emitter structure, the concentration of the base 6 at a portion directly under the emitter 9 is high, and thereby an emitter-base withstand voltage is

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determined at this portion, thus obtaining only a withstand voltage from 2 to 4 V.

To apply such a bipolar transistor to TTLI/0 or the like, an emitter-base withstand voltage of about 3.5 V or more is required. Therefore, in general, the emitter-base withstand voltage is required to be ensured by increasing an ion implantation energy upon formation of the base 6 (see Fig. 4C) for reducing an impurity concentration of the base at the emitter-base junction. --

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Please replace the paragraph beginning at page 6, line 1, with the following rewritten paragraph:

-- A semiconducting substrate; a first impurity diffusion layer having a first conducting type, which is formed in the semiconducting substrate; --

Please replace the paragraph beginning at page 14, line 7, with the following rewritten paragraph:

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-- FIGs. 1A, 1B and FIGs. 2A, 2B are process diagrams illustrating a method of fabricating a bipolar transistor of the present invention. These figures are sectional views showing the upper side of a substrate, particularly,

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an emitter portion and a base portion of an npn-transistor.

First, like the prior art method shown in FIGs. 4A and 4B, a SiO₂ film 2 (thickness: 100 to 200 nm) having opening side walls 2a and a p-type poly-Si film 3 (thickness: 100 to 200 nm) are formed on a silicon substrate 1 as a semiconducting substrate. Then, as shown in FIG. 1A, a SiO₂ film 4 having a thickness of from 300 to 400 nm is formed on the poly-Si film 3 by CVD. Then, an opening 10 for forming an emitter and a base is formed by etching (RIE) of the SiO₂ film 4 and the poly-Si film 3. A SiO₂ film 5 having a thickness of from 10 to 20 nm is formed over the surface by CVD, and then a p-type impurity diffusion layer 11 is formed by ion implantation under a condition specified by the present invention. The p-type impurity diffusion layer 11 serves as a link base layer. It is to be noted that the thin SiO₂ film 5 serves a buffer layer for preventing the channeling tail upon ion implantation for forming the link base layer. --

Please replace the paragraph beginning at page 15, line 9, with the following rewritten paragraph:

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--The ion implantation condition for forming the p-type impurity diffusion layer (link base layer) 11 is as follows:

implanted ion: BF_2

energy: 5-20 KeV

dose: $1 \times 10^{12} - 1 \times 10^{14} \text{ cm}^{-2}$

diffusion depth of link base layer: 30 to 50 nm. --

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Please replace the paragraph beginning at page 15, line 13, with the following rewritten paragraph:

--The ion implantation of BF_2 at a low energy of from 5 to 20 KeV is equivalent to the ion implantation of B (boron) at a low energy of from 1 to 5 KeV. --

Please replace the paragraph beginning at page 15, line 21, with the following rewritten paragraph:

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--After the link base layer 11 is formed by ion implantation of BF_2 , as shown in FIG. 1B, ions of a p-type impurity such as boron (B) are implanted in a dose of from 1×10^{12} to $1 \times 10^{14} \text{ cm}^{-2}$ at an energy of from 10 to 100KeV, to form a base 12 as a p-type impurity diffusion layer. --

Please replace the paragraph beginning at page 16, line 9, with the following rewritten paragraph:

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--With the above-described sequential processes, (1) the concentration of the base 12 (including the link base layer 11) at a portion directly under the side wall 7a isolates the emitter from the base without any increase in the base concentration at a portion directly under the emitter, thus preventing variations in characteristics due to variations in a correct current or the base recombination current at such a portion, and ensuring reliability; and (2) an increase in the thickness of the base 12 is suppressed. --

Please replace the paragraph beginning at page 16, line 19, with the following rewritten paragraph:

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--After that, as shown in FIG. 2A, heat-treatment (annealing) is performed for 10 to 20 minutes at 900°C, to diffuse the p-type impurity from the p-type poly-Si film 3 to the Si substrate, thus forming a P⁺ contact layer 3a. The p⁺ contact layer 3a serves as a graft base. In addition, the heat-treatment may be shared with the heat-treatment for emitter diffusion which will be performed